SILICON LABS

AN577

Si4010 NVM Read Reliability Analysis

1. Introduction

The purpose of this document is to describe the long term reliability of the One-Time-Programmable Non-Volatile-Memory (NVM) block of the Si4010.

When starting up the Si4010 (i.e., power up or reset), a boot process occurs during which the NVM is read and copied into the RAM. Assuming a standard mode of operation, the number of NVM reads is much less than the maximum number of read cycles the NVM can withstand, thus there is no customer issue. The NVM in a typical use case can withstand on the order of 7E9 accesses. However, there can be special cases when the user application needs to access the NVM not only upon the boot process, but during runtime as well. Using the memory overlay technique or keeping data (e.g., security keys) in the NVM, which is not loaded upon boot, may result in more NVM reads than usual and, therefore, the long-term reliability of the NVM must be considered. However, it should be noted that only extreme parameters could result in a reduced lifetime of the NVM as the examples demonstrate in Section 2.

The most common application of the Si4010 is a keyfob transmitter in RKE systems, and the typical usage profile of the keyfob includes less then 100 button presses per day. The calculations in Section 2 show that the Si4010 can support applications requiring 10000 times bigger number of operations.

2. Reliability Analysis

To calculate the NVM reliability, the read time must be calculated with each startup of the device from the shutdown state or when either a memory overlay page or external data is swapped from the NVM into RAM.

The memory reliability is dependent on several factors including the read voltage, temperature, and amount of memory used in the customer's application. In the Si4010, the NVM block is read using a constant, regulated 2.7 V regardless of the applied V_{DD} to the device, so this parameter can be considered invariant in all reliability calculations.

Table 1. NVM Block Characterization Data

Parameter	Description	Value
Cumulative Read Time	125 °C, 0.1% single-bit failure rate, 2.7 V read voltage, allowed cumulative read time	5.35E7 seconds
	25 °C, 0.1% single-bit failure rate, 2.7 V read voltage, allowed cumulative read time	2.71E8 seconds
Temperature Variation	Increase in cumulative read time for single-bit failure with temperature decrease	1.5 / 25 °C
Failure Rate Scaling	Decrease in cumulative read time for single-bit failure with each 10x failure rate decrease	1 / 5.5
Bit Access Time	Average time per NVM bit access	550 ns

In normal operation, the NVM is read during boot up and copied into the Si4010 RAM. The Si4010 MCU does not execute code directly out of the NVM. Therefore, when calculating the NVM reliability, the read time is only required to be calculated with each startup of the device from the shutdown state or when a memory overlay page is swapped from the NVM into RAM.

Copyright © 2011 by Silicon Laboratories

Based on the fab characterization of the NVM block, a 0.1% failure probability of a single bit at 125 °C requires a cumulative read time of 5.35e7 seconds (or 620 days) at 2.7 V (see Table 1). For each 25 °C drop in temperature, the read time increases by 1.5x. For example, at 25 °C ambient temperature, the cumulative time to achieve this error rate increases by a factor of 5 as shown below:

$$Temp_{Delta} = 125°C - 25°C = 100°C$$

$$Scaling_{Factor} = 1.5 \wedge \frac{100°C}{25°C} = 5.06$$

The cumulative read time at 25 °C increases to 5.35e7 seconds x 5.06 = 2.71e8 seconds (or 3137 days) at 25 °C for a 0.1% failure probability of a single bit.

In order to calculate the overall failure rate of the NVM array, the single-bit failure rate needs to be extended to include the entire memory. For example, the probability of NVM failure is equal to the single-bit failure rate scaled by the NVM array size. The entire Si4010 NVM memory size is 8 k bytes or 65535 bits. In this analysis, we assume that on boot, only half the NVM could be read because the RAM is approximately 4 k bytes. For example, if the overall NVM failure rate is to be 10 ppm, then the probability of any single bit failing in the NVM array during boot is:

$$\frac{10\text{ parts}}{1E6} \times \frac{1}{32768\text{ parts}} = 3.05E\text{-}10$$

If the memory size loaded during boot is smaller than 32768, this probability should be recalculated with the actual memory used.

Note that, in this application note, we calculate both logic \`0\`s and logic \`1\`s as potentially misread bits due to the cumulative read time stress. This is a very conservative estimate. In reality, only the unburned bits, logic \`0\`s, are affected since the cumulative failure mode results in a logic '0 being misread as a logic '1. When determining the number of potential bits failing, 32768 in our example, this could be taken into account by applying a factor. For instance a factor of 0.5 would assume that half of the bits are logic \`0\`s.

In order to determine a single-bit failure rate other than 0.1%, there is a decreased read time of 5.5x for every 10x decrease in probability. For example, to extrapolate single-bit read time failure rates from 1e-3 (0.1% single bit failure rate) to 3.05e-10 (corresponding to the NVM overall failure rate of 10 ppm) the single-bit read time needs to be reduced by a factor of:

$$5.5^{\log 10\left(\frac{1E-3}{3.05E-10}\right)} = 6.67E4$$

So, the cumulative single-bit read time of any bit in the 32768 bit cells accessed during boot that yields an overall 10 ppm NVM failure rate at 25ºC can be calculated as:

$$\frac{2.71E8\text{ seconds}}{6.67E4} = 4060\text{ seconds}$$

Since the average read time is 550 ns per bit, the number of button presses the Si4010 application can support to achieve a 10 ppm error rate at 25 ºC using the 32768 bits accessed on boot is:

$$\frac{4060\text{ seconds}}{550E-9\text{ seconds}} = 7.49E9\text{ button presses}$$

SILICON LABS

Another way to calculate this number is to consider the total lifetime of the device and determine how frequently a button can be pushed to achieve this error rate. For example, if the desired product lifetime is 10 years, the device can support:

$$\frac{7.4E9 \text{ button presses}}{10 \text{ years} \times \frac{365 \text{ days}}{\text{year}} \times \frac{24 \text{ hours}}{\text{day}} \times \frac{60 \text{ minutes}}{\text{hour}}} = 1408 \text{ presses per minute}$$

So far, the usage model assumes we are reading half the NVM each time a button is pressed, executing the loaded application in RAM, and then going back to sleep. When using RAM overlays to swap multiple NVM pages into the RAM, individual bits in the NVM block can be accessed more than once per button press. The total number of memory overlays and their size as well as the total number of NVM accesses needs to be estimated to calculate the resulting NVM reliability. To do this, define a variable M equal to the average size of each memory overlay in the application. M is expressed as a percentage of the overall size of the NVM. For instance, if the application requires three overlays comprising the entire NVM, then M = 1/3. In addition, define a variable N equal to the total number of overlays called by the application.

$$\text{Average Read Time} = \text{Avg Time due to Boot} + \text{Avg Time due to Overlays}$$

$$\text{Average Read Time} = 550 \text{ ns} \times N_B \times M_B + 550 \text{ ns} \times N_O \times M_O$$

For this example, assume that the application boots once per button press (reading half the memory, so $M_B = ½$ and $N_B = 1$ for boot), and then reads the entire memory once again using two memory overlays to execute the application (so $M_O = ½$ and $N_O = 2$ to execute the application). The new average read time for each bit in the NVM can now be calculated using this equation:

$$\text{Average Read Time} = 550 \text{ ns} \times 1 \times \frac{1}{2} + 550 \text{ ns} \times 2 \times \frac{1}{2} = 825 \text{ ns}$$

The probability of a single-bit failure with an overall NVM failure rate of 10 ppm needs to be calculated over the entire 65535 bit memory and used to scale the 0.1% probability rate to calculate the cumulative read time:

$$\text{Single Cell Failure Probability (@ 10 ppm)} = \frac{1}{1E6} \times \frac{1}{65535} = 1.52E-10$$

$$\text{Scaling Factor from 0.1\% failure rate} = 5.5^{\log 10\left(\frac{1E-3}{1.526E-10}\right)} = 1.11E5$$

$$\text{Cumulative Read Time} = \frac{2.71E8 \text{ seconds}}{1.11E5} = 2440 \text{ seconds}$$

Converting this number into a total number of button presses per minute for a 10 year lifetime results in:

$$\text{Button Presses} = \frac{2440 \text{ seconds}}{825E-9 \frac{\text{seconds}}{\text{button press}}} = 2.96E9$$

$$\frac{2.96E \text{ button presses}}{10 \text{ years} \times \frac{365 \text{ days}}{\text{year}} \times \frac{24 \text{ hours}}{\text{day}} \times \frac{60 \text{ minutes}}{\text{hour}}} = 562 \text{ button presses per minute}$$

In order to determine the actual failure rate for a specific customer application, the nature of the memory overlays needs to be calculated as illustrated above for the specifics of that application. The same method should be applied when data is stored in the NVM, which is not copied to the RAM upon boot, but read multiple times during runtime.

Simplicity Studio

One-click access to MCU tools, documentation, software, source code libraries & more. Available for Windows, Mac and Linux!

www.silabs.com/simplicity

MCU Portfolio
www.silabs.com/mcu

SW/HW
www.silabs.com/simplicity

Quality
www.silabs.com/quality

Support and Community
community.silabs.com

Disclaimer
Silicon Laboratories intends to provide customers with the latest, accurate, and in-depth documentation of all peripherals and modules available for system and software implementers using or intending to use the Silicon Laboratories products. Characterization data, available modules and peripherals, memory sizes and memory addresses refer to each specific device, and "Typical" parameters provided can and do vary in different applications. Application examples described herein are for illustrative purposes only. Silicon Laboratories reserves the right to make changes without further notice and limitation to product information, specifications, and descriptions herein, and does not give warranties as to the accuracy or completeness of the included information. Silicon Laboratories shall have no liability for the consequences of use of the information supplied herein. This document does not imply or express copyright licenses granted hereunder to design or fabricate any integrated circuits. The products must not be used within any Life Support System without the specific written consent of Silicon Laboratories. A "Life Support System" is any product or system intended to support or sustain life and/or health, which, if it fails, can be reasonably expected to result in significant personal injury or death. Silicon Laboratories products are generally not intended for military applications. Silicon Laboratories products shall under no circumstances be used in weapons of mass destruction including (but not limited to) nuclear, biological or chemical weapons, or missiles capable of delivering such weapons.

Trademark Information
Silicon Laboratories Inc., Silicon Laboratories, Silicon Labs, SiLabs and the Silicon Labs logo, CMEMS®, EFM, EFM32, EFR, Energy Micro, Energy Micro logo and combinations thereof, "the world’s most energy friendly microcontrollers", Ember®, EZLink®, EZMac®, EZRadio®, EZRadioPRO®, DSPLL®, ISOmodem ®, Precision32®, ProSLIC®, SiPHY®, USBXpress® and others are trademarks or registered trademarks of Silicon Laboratories Inc. ARM, CORTEX, Cortex-M3 and THUMB are trademarks or registered trademarks of ARM Holdings. Keil is a registered trademark of ARM Limited. All other products or brand names mentioned herein are trademarks of their respective holders.

Silicon Laboratories Inc.
400 West Cesar Chavez
Austin, TX 78701
USA

http://www.silabs.com